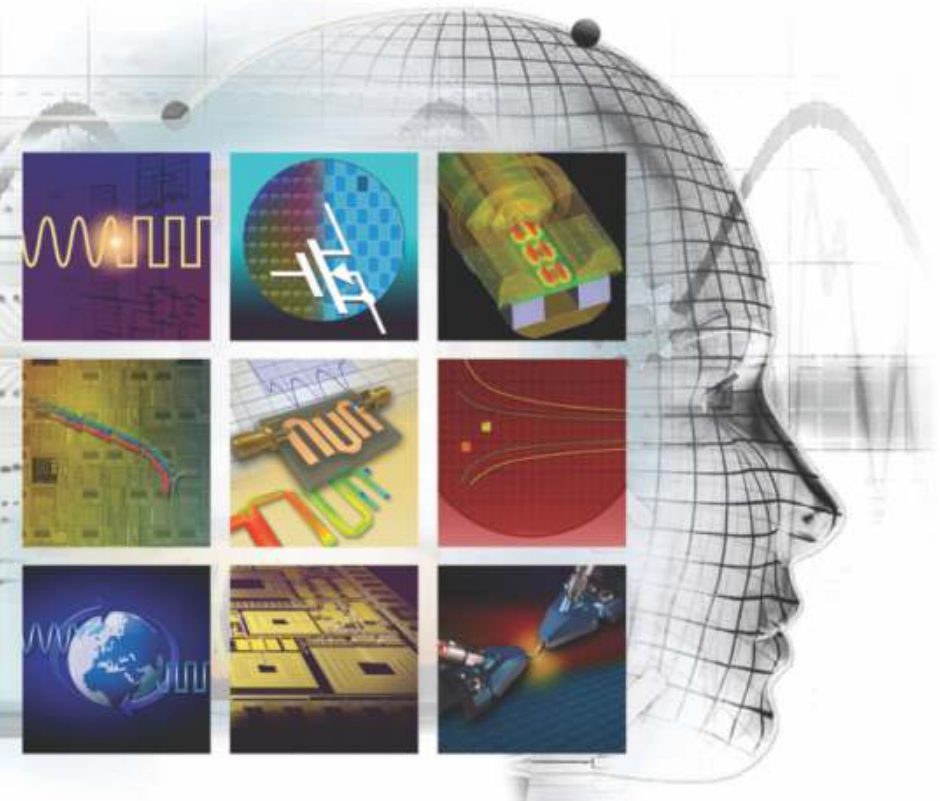
Keysight India 2017
EEsof Design Forum

Unlock your 'Design to Test' insights.
Move the technology forward. Faster.



Hyderabad October 24 | **Bengaluru** October 26 | **Ahmedabad** October 28

KEYSIGHT TECHNOLOGIES

Agilent's Electronic Measurement Group is now **Keysight Technologies**.

Keysight India 2017
EEsof Design Forum

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Keysight's Advanced Design System is the world's leading electronic design automation software for RF, microwave, and high speed digital applications. In a powerful and easy-to-use interface, ADS pioneers the most innovative and commercially successful technologies, such as X-parameters and 3D EM simulators, used by leading companies in the wireless communication & networking and aerospace & defense industries. For WiMAX, LTE, multi-gigabit per second data links, radar, & satellite applications, ADS provides full, standards-based design and verification with Wireless Libraries and circuit-system-EM co-simulation in an integrated platform.

Keysight India 2017 EEsof Design Forum is a unique platform to unlock your 'Design to Test' insights. As a developer, you will get to know how Keysight can help you solve the design and test challenges you face while developing tomorrow's advanced technologies. Learn how you can build an integrated and collaborative design environment, work synergistically to accelerate time to market and optimize your designs utilizing both hardware and software.

Who Should Attend : RF/MW, EM, Baseband System Architects, Digital Application Designers, Software developers and Hardware Engineers.

What to expect in ADS 2017 & EMPro 2017: 3D Design, 3D Simulation and 3D Data Visualization

With the new release of ADS 2017, Keysight is building upon their industry leading RF/MW circuit simulation software platform with improvements in customer experience (3D Viewer, Quickstart Guide, Python Data Link) and performance (circuit and FEM simulation speed, handling complex layouts, multi-technology support). This together with many other new features help to make the life easier for those who do both RF Front-end module and RFIC silicon design. Also with the new release of EMPro Keysight continues to be a leading 3D electromagnetic modeling and simulation environment, which is also integrated with the ADS design flow. This release offers a number of new capabilities to reduce simulation time (FEM performance improvements, easier to use Python scripting, adaptive meshing) and increase design efficiency (improved parameterization, FEM native field visualization).

New Features in SystemVue

Phased Array Antenna & pre-5G Design : SystemVue 2017 Electronic System Level (ESL) simulation software enables the industry's first 5G link level validation with RF phased array beamforming in mm wave channel environments that is required for 5G standards compliance, but also applicable to other type of phased array systems for example in automotive and other radar systems.

When & Where

Tuesday, October 24
Hotel Taj Deccan,
Banjara Hills,
Hyderabad

Thursday, October 26
Hotel Vivanta by Taj,
MG Road,
Bengaluru

Saturday, October 28
Hotel Novotel,
ISKCON Cross Road, S.G. Highway.
Ahmedabad

AGENDA

OCTOBER 24 | HYDERABAD

TIME	TOPIC	PRESENTER
09.00-09.30	Registration	
09.30-09.45	Introduction & Welcome	*Deepak R.K*
09.45-10.30	What's New – Keysight EEsof EDA (ADS2017, SystemVue2017 and EMPro2017)	*Anurag Bhargava*
10.30-11.15	**KP2:** Virtual Flight Testing of Radar System – SystemVue & AGI STK	*Pratik Khurana (Keysight) & Libish Balachandran (AGI)*
11.15-11.30	**Tea Break**	
11.30-12.15	**KP1:**DC-DC Converters: Understanding & Controlling Conducted Emissions	*Anurag Bhargava*
12.15-13.00	**KP3:** Design and Analysis of Passive Components and Transmission Lines using **CoilSys** in ADS2017	*K. Chan Basha (Keysight R&D)*
13.00-13.45	**LUNCH**	
13.45-14.30	**CP1:** Latest improvements in modeling for GaN & GaAs foundry processes with the support of ADS capabilities	Philippe Michel, Head - UMS Modeling group
14.30-15.00	**CP2:** Design of 20W X-band MMIC Amplifier	Bhupinder Singh, FineTuningRF
15.00-15.30	**CP7:** Design & Development of reconfigurable pre-selector using switched multiplexer for hybrid receiver application	*Manish Mendhe, DLRL*
15.30-16.00	**CP8:** Two stage Ka-Band LNA using BiCMOS technology	*Divya Kumar Garg, ANURAG*
16.00-16.30	**CP9:** Design and simulation of pHEMT based 0.5-20 GHz LNA using cascode cell configuration	*Manish Mendhe, DLRL*
16.30-16.45	**Tea Break**	
16.45-17.00	**Closing & Lucky Draw**	

OCTOBER 26 | BENGALURU

TIME	TOPIC		PRESENTER
08.45-09.15	Registration		
09.15-09.30	Introduction& Welcome		*Deepak R.K*
09.30-10.15	What's New – Keysight EEsof EDA (ADS2017, SystemVue2017 and EMPro2017)		*Anurag Bhargava*
10.15-11.00	**KP1:**DC-DC Converters: Understanding & Controlling Conducted Emissions		*Anurag Bhargava*
11.00-11.15	**Tea Break**		
	RF/Microwave Track (T1)	**High Speed Digital (T2)**	
11.15-12.00	**KP2:** Virtual Flight Testing of Radar System – SystemVue & AGI STK – *Pratik Khurana (Keysight) & Libish Balachandran (AGI)*	11.15-12.15	**Live Demo:** ADS2017 enhancements for HSD applications a. New IBIS Parser & Use model b. Auto Wire Connections c. IR Drop with Electrothermal d. PAM4 Statistical Simulations – *Anurag Bhargava*
12.00-12.45	**KP3:**Design and Analysis of Passive Components and Transmission Lines using **CoilSys** in ADS2017 – *K. Chan Basha (Keysight R&D)*	12.15-12.45	**KP5: PCI Gen4:** How Long Bit can travel before it needs to refuel? – *Amit Jangale (Keysight R&D)*
12.45-13.30	**LUNCH**		
13.30-14.15	**CP1:** Latest improvements in modeling for GaN & GaAs foundry processes with the support of ADS capabilities – *Philippe Michel, Head - UMS Modeling group*	13.30-14.15	**Live Demo:** Design, Parameterize & Analyze 3D VIAs with great ease using **VIA Designer** in ADS2017 – *Shobhit Tiwari (Keysight R&D)*
14.15-14.45	**CP2:** Design of 20W X-band MMIC Amplifier – *Bhupinder Singh, Fine Tuning RF*	14.15-15.15	**KP4: Case Study:** Signal and Power Integrity Analysis of a DDR4 board – *Anurag Bhargava*
14.45-15.15	**CP3:** Sea Eagle Navigation Radar – System Design – *M. Janakiraman, Independent Consultant*	15.15-15.45	**CP10:** Pattern Effects in PCIe Gen3 Compliance Results – *Surjendra Goswami, Seagate, Bangalore*
15.15-15.45	**CP4:** Compact 0.5-40 GHz Microstrip Power Divider Design – *Rohit Lahiri, BEL-Bangalore*		
15.45-16.15	**CP5:** Design of S-band Interdigital Bandpass Filter – *Rahul Sadhu, BEL-Bangalore*	15.45-16.15	**CP6:** Significance of Simulations in High Speed Designs – *M.P.V. Bhaskara Rao, CDOT - Bangalore*
16.15-16.30	**Tea Break**		
16.30-16.45	**Closing & Lucky Draw**		

OCTOBER 28 | AHMEDABAD

TIME	TOPIC	PRESENTER
09.00-09.30	Registration	
09.30-09.45	Introduction& Welcome	*Deepak R.K*
09.45-10.30	What's New – Keysight EEsof EDA (ADS2017, SystemVue2017 and EMPro2017)	*Anurag Bhargava*
10.30-11.15	**KP3:** Design and Analysis of Passive Components and Transmission Lines using **CoilSys** in ADS2017	*K. Chan Basha (Keysight R&D)*
11.15-11.30	**Tea Break**	
11.30-12.15	**KP1:** DC-DC Converters: Understanding & Controlling Conducted Emissions	*Anurag Bhargava*
12.15-13.00	**CP1:** Latest improvements in modeling for GaN & GaAs foundry processes with the support of ADS capabilities	*Philippe Michel, Head - UMS Modeling group*
13.00-13.45	**LUNCH**	
13.45-14.30	**KP6:** Signal Integrity and Power Integrity Analysis using ADS	*Pratik Khurana*
14.30-15.15	**KP7:** ADS - Cadence Virtuoso Interoperability & Momentum in Virtuoso with ADS2017	*Anjali Arora (Keysight R&D)*
15.15-16.30	**KP8:** 4 ways to Boost ADS Simulation Data Processing using Python	*Anurag Bhargava*
16.30-16.45	**Tea Break**	
16.45-17.00	**Closing & Lucky Draw**	

PAPER OVERVIEW

Keysight Papers

KP1: DC – DC Converters: Understanding & Controlling Conducted Emissions

Anurag Bhargava, Application Consultant

High speed power converters produce noise and EMI that can interfere with other electronics and degrade performance and/or reliability. While Radiated Emission are something to pay attention to, the frequency of operation is not typically in the communication bands. This coupled with the fact that the physical size of a SMPS is less than the wavelength of a communications band frequency, means that radiation emissions are typically not as big a concern as conducted emissions which can disrupt products through a conduction or capacitive coupling mechanism. Using modern, integrated EDA toolsets, conducted emissions can be easily simulated and compliance predicted up front using an EMC design process.

Hyderabad, Bengaluru, Ahmedabad

KP2: Virtual Flight Testing of Radar System – SystemVue and AGI STK

Pratik Khurana (Keysight) & Libish Balachandran (AGI)

The costs of flight testing of Radar systems using real aircraft can be over $100,000 per hour and the results from one run to the next are not repeatable. By combining the capabilities of two software tools namely Keysight SystemVue and AGI STK, complex Radar systems can be evaluated hundreds of times in an hour, using the same or different scenarios for each run, and at significantly less cost than a single hour on a flight range.

Keysight's SystemVue will be used to model the Radar System including waveform generation, transmitter and receiver non-ideal behavior of components and radar post-processing. Analytical Graphics Inc's STK software will be used to model the flight scenario and the characteristics of the signal path(s) including Path Loss, Doppler, aircraft aspect Radar Cross Section, atmospheric losses, etc. Radar acquisition, avoidance and jamming in dynamic "real-world like" scenarios will be presented.

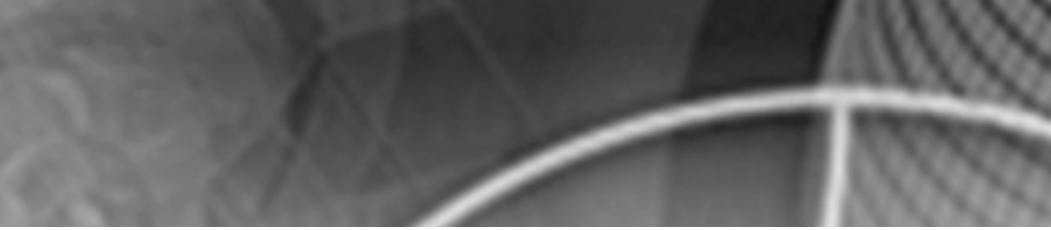
Hyderabad, Bengaluru

KP3: Design and Analysis of Passive Components and Transmission Lines using CoilSys in ADS2017

K. Chan Basha, Keysight R&D

The foundries typically provide PDKs with a basic set of passive devices that can respond to user's input of physical parameters. The on-chip passive components are necessary and imperative adjuncts to most RF electronics including inductors, capacitors, transformers, and resistors. Inductors are particularly critical components in low noise amplifiers, oscillators and other tuned circuits. The inductors are large and occupies an expensive chip space. With ADS Momentum, one can EM simulate an RFIC inductor if the layout already exists, but how to design the best possible layout? How to find the best inductor layout for designer requirements? In RF/microwave circuit design, inductor design is one of the most difficult and time-consuming tasks due to the tedious trial-and-error optimization process to achieve the target specifications such as inductance, quality factor and SRF.

This paper summarizes the design and analysis of various types of passive components (Inductors, Baluns/Transformers and Solenoid) and Transmission Lines using Coilsys in ADS2017. CoilSys is an application level add-on utility in ADS2017 that creates DRC clean component layouts, whose layers



are mapped to a Momentum substrate in ADS. These layouts can be tuned/parameterized and EM simulated. It also generates scalable EM model through Advanced Model Composer. It creates the required PCells (ItemDef based and CDF based) in PDK which are not always available. It creates the add-on Library package for ADS flow and Virtuoso flow and also it enables designer to get an optimized inductor design quickly, without involving "time consuming" trial-and-error EM simulation.

Hyderabad, Bengaluru, Ahmedabad

KP4: Case Study – Signal & Power Integrity Analysis of DDR4 board

Anurag Bhargava, Application Consultant

This paper presents complete case study of performing Signal and Power Integrity for a DDR4 board. We shall showcase complete simulation flow including DC IR Drop analysis, PDN analysis, Data Lane, Address Bus SI analysis etc along with SSN and Power Aware SI analysis alongwith BER simulations as recommended in JEDEC standardfor Xilinx Kintex KCU 105 board.

Bengaluru

KP5: PCIe Gen4 – How long Bit can travel before it needs to refuel?

Amit Jangale, Keysight EEsof R&D

This paper presented End-to-End System Simulation for PCIe Gen4 to gain confidence in the chosen topology and it viability. We shall discuss about need of using repeater, defining a simulation space, determine evaluation criteria and execute the simulation matrix and analyze the result to reach a conclusion regarding the optimum configuration of the system in an efficient and timely manner. Also, we shall perform sensitivity analysis to decide the optimum location of the repeater followed by a case study of Simulation vs. Measurement using an Analog Bits PCIe Gen4 Test Chip.

Bengaluru

KP6: Signal and Power Integrity Analysis with ADS

Pratik Khurana, Application Engineer

Signal Integrity and Power Integrity continue to pose challenges for Digital Engineers. With clock frequencies and data rate continuing to rise, maintaining signal and power quality is becoming lot more challenging. Traditional SI &PI tools lack capability to accurately handle high frequency effects on the digital & clock signals. SIPro and PIPro modules in ADS offers great ease-of-use and very accurate set of simulators to perform Signal and Power Integrity analysis. This presentation provides overview of SIPro & PIPro simulators in ADS alongwith many simulated vs. measured case studies.

Ahmedabad

KP7: ADS - Virtuoso Interoperability & Momentum in Virtuoso with ADS2017

Anjali Arora, Keysight EEsof R&D

This paper presents some of the significant improvements for RFIC design flow with ADS2017 release. We shall provide overview of RFIC solutions offered by Keysight followed by various live demos covering:

a. ADS – Virtuoso Interoperability
b. Automatic EM-Cosimulation
c. Momentum in Virtuoso
d. Package Simulations

Ahmedabad

KP8: 4 ways to Boost ADS Simulation Data Processing using Python

Anurag Bhargava, Application Consultant

The solution to most of engineering problems can be found somewhere in the data available however, huge amount of multi-dimensional data which needs to be processed to extract the desired information is not an easy task by any means. This paper present a new & practical approach of using Python scripting which is open source and freely available for anyone wanting to use it with Keysight ADS with simple setup to perform deep data mining or to create various kind of 3D plots with great ease.

We shall present 4 different type of case studies to give in-depth ideas to the designers:

a. Designing a Broadband Amplifier with a 3D Smith Chart (Smith Tube)
b. De-embedding measured load pull data using EM analysis of fixture
c. Synthesizing an Acoustic Filter by a residual extraction technique
d. PAM-4 simulation to measurement validation on DCA Oscilloscope

Ahmedabad

Customer Papers

CP1: Latest improvements in modeling for GaN & GaAs foundry processes with the support of ADS capabilities

Philippe Michel, Head - UMS Modeling group

Availability of accurate electrical models is a prerequisite for high performance MMIC design and successful first GaAs and GaN foundry run. UMS European foundry offers a large panel of GaAs processes (Schottky, MESFET, 0.25µm or 0.15µm pHEMTs, HBT) but also a 0.25µm AlGaN/GaN HEMT. Providing accurate scalable models and useful PDKs is essential for successful design. ADS from Keysight allows simulation of active device behaviours and permits accurate E/M simulation of passive elements. Brief description of the different complex behaviours, such as frequency dispersive effects, nonlinearity, thermal dependence, noise, will be presented with GaN and GaAs examples. Also, we shall present experimental validation of model through real cases.

Hyderabad, Bengaluru, Ahmedabad

CP2: Design of a 20W X-Band MMIC

Bhupinder Singh, Fine Tuning RF

The design of an X-Band MMIC is presented using a .25micron GaN/SiC process. Extensive EM simulation and compact circuit design techniques were utilized to realize MMIC on a 5mmX5mm die size. Layout features in ADS along with EM simulation were used in the design of the MMIC. The simulation results show more than 20W power out and greater than 22db of small signal gain

Hyderabad, Bengaluru

CP3: Sea Eagle Navigation Radar

M. Jankiraman, Independent Consultant

This presentation deals with a fictitious marine navigation radar system. The specifications of this radar are contemporary. The presentation opens with a brief appraisal of Frequency Modulated Continuous Wave (FMCW) radars, its advantages and disadvantages. It then lists out the desired specifications of

the Sea Eagle radar and then goes on to achieve it. The radar is configured in a homodyne configuration. This radar is fully MTD (Moving Target Detector) radar and the display is on the Doppler plane.We then discuss the hardware realization and then carry out live simulations using SystemVue.

Bengaluru

CP4: Compact 0.5-40 GHz Two Way Symmetric Microstrip Power Division Circuit

Rohit Lahiri. Microwave Components, Central- D&E, Bharat Electronics Limited - Bangalore

An ultra-wide band 0.5-40 GHz compact three port power divider design and development procedure is explained. The challenges of multi section power divider design is to provide enough input matching compared to output port matching, as output port can be balanced by inter connecting resistors. This design includes single T-junction of three transmission lines and series of cascaded uncoupled quarter wave transmission line sections at its centre frequency that are connected by discrete wide band resistors. This design achieves minimum usable bandwidth of f2/f1=1.75:1 with peak VSWR 1.9:1 in band. It is also observed that the operating bandwidth achieved in the simulation is slightly broader than the theoretical calculations. Modelling and simulations has been carried out in Advanced Design System (ADS), both in schematic and momentum platforms, and practical results achieved are satisfactorily meeting simulated results. This power divider design is realised in micro-strip layout featuring a significant amount of robustness, allowing for a large amount of freedom and flexibility for its realisation. It can be used as a drop in module, as a packaged module or as a part of circuit. This design can be used for any wide band systems in such as receivers, LO distribution projects, transmitters, testing modules, Built In Test Equipment (BITE) modules etc.

Bengaluru

CP5: Deign of S-Band Interdigital Band Pass Filter

Rahul Sadhu, Central D&E, Bharat Electronic Limited - Bangalore

A Band Pass Filter is one of the key components in the receive chain of any Transmit-Receive Module of an Active Array Radar. The critical parameter for the design of a BPF for a TR module is the form factor,insertion loss and rejection. Hence a microstrip based interdigital (tapped) BPF for S-Band TR Module (3.1-3.5 GHz) was designed. The filter was designed to achieve a typical insertion loss of 2.0 dB in the passband and a rejection of 50 dB on either side at 1.2 GHz away from centre frequency. The filter was realized and tested successfully on a 25 mil thick Rogers's substrate having a dielectric constant of 10.2. Further development is under progress to suppress the harmonics.

Bengaluru

CP6: Significance of Simulations in High Speed Designs

MPV Bhaskara Rao, CDOT - Bangalore

Performing accurate simulations are critical to the first pass success in High Speed Design as the design space is quite big and margins are usually quite small. This paper presents various design exploration techniques which can be performed to create a successful methodology for a High-Speed Board design. Two case studies will be presented:

a. How Pre-Layout simulation helped us to select a device
b. How Post-Layout simulations helped us to optimize the high-speed channel

Bengaluru

CP7: Design and development of reconfigurable pre-selector using switched multiplexer approach for hybrid receiver application

Manish Mendhe, DLRL, Hyderabad

A reconfigurable pre-selector covering 2-18 GHz has been designed to meet the hybrid receiver requirement. it consists of 4 channel input multiplexer (contiguous) with crossover frequencies at 6,10 and 14 GHz, output multiplexer (contiguous) with crossover frequencies at 4,8.12 and 16 GHz and channel control module which has 8 SPST switches with power divider and power combiner. The reconfigurable pre-selector can be configured to have 2^8 combinations of the bandwidths.

Hyderabad

CP8: A two stage Ka-Band LNA using BiCMOS technology

Divya Kumar Garg, ANURAG, Hyderabad

This paper presents the two-stage single ended low noise amplifier at Ka-band using Virtuoso-Momentum tool. The LNA is based on a 0.13 um SiGe heterojunction bipolar transistor process for AESA radar application. Virtuoso -Momentum EM tool from Keysight has been used within Virtuoso design flow instead of virtuoso extraction tool. Self-designed inductors, synthesized by EM tool has been used instead of foundry provided inductor Pcells. The measured gain at Ka-band is 20dB, and with a noise figure of 3.9dB. The two stage LNA consumes 8.1 mW (4.5mA , 1.8V) and the input 1-dB gain compression point is -27dBm. The chip size is less than 0.5 mm2 without pads.

Hyderabad

CP9: Design and simulation of pHEMT based 0.5-20 GHz LNA using cascode cell configuration

Manish Mendhe, DLRL, Hyderabad

The ultrawideband LNA covering 0.5-20 GHz is designed and simulated using OMMIC pHEMTPDK. The casocde cell topology is used for distributed configuration instead of conventional single transistor version to enhanced the stability, reverse isolation and gain at higher frequencies. the EM simulated gain achieved is 19.5 +/-1 dB, with noise figure less than 2 dB from 2-20 GHz and 4 dB max from 0.5-2 GHz. input output matching is better than 15 dB with reverse isolation better than 35 dB

Hyderabad

CP10: Pattern Effects in PCIe Gen3 Compliance Results

Surjendra Goswami, Seagate, Bangalore

The PCIe Gen3 compliance requires a specific pattern for the compliance measurements for the Receiver and the Transmitter. However, this is not the standard pattern used during the simulations. As a result, there is a difference between the compliance measurements in the lab and simulation environments. This paper elaborates the methodology for the PCIe Gen3 compliance and measurements for the Transmitter and quantifies the difference in the observed results. It also discusses the Infiniium Scope software utility in ADS for compliance related measurements.

Bengaluru

Keysight India 2017 EEsof Design Forum

REGISTRATION FORM

There is no charge for this seminar, but seating is limited and early registration is recommended.

To register

- Please call: 1800 11 2626 (Toll free) or 0124 229 2010
- Fax: 1800 11 3035 (Toll free) or 0124 229 2011
- email: tm_india@keysight.com

Date & Place :

- ○ Tuesday, 24th October 2017 | Hotel Taj Deccan, Banjara Hills, Hyderabad
- ○ Thursday, 26th October 2017 | Hotel Vivanta by Taj, MG Road, Bengaluru
- ○ Saturday, 28th October 2017 | Hotel Novotel, ISKCON Cross Road, S.G. Highway. Ahmedabad

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If you wish to invite your colleague, please share his details:

NAME : _____

JOB TITLE : _____

COMPANY : _____

DEPARTMENT : _____

ADDRESS : _____

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KEYSIGHT TECHNOLOGIES

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